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(54) **Infrared imaging devices**

(57) In an infrared imaging device, photocurrent generated by detector elements 1, e.g. cadmium mercury telluride photodiodes, is integrated in resettable capacitors 2, and an output signal S is derived by reading the potential of the capacitor 2 at the end of its integration period, e.g. using a source-follower MOST 3. In accordance with the invention, the addressing and switching means 6, 7 of the device sequentially couples each capacitor 2 to a common reading means 3, and a common reset means 5 resets sequentially the reference voltage level at each capacitor 2 and at the common voltage-reading means 3. This avoids non-uniformities in detector element signal processing and measurement which can arise with each capacitor 2 having individual voltage reading means and reset means. It also provides a compact cell structure and suitable circuit configuration for enhancing the device performance, for example by adding blooming-protection means 11 and/or an expanded capacitor arrangement for increasing or varying the integration capacity and/or for providing alternatively switchable integration means for each detector element 1, and/or for interfacing with a 2-d switched array of detector elements 1. Preferably, a shift register 6 with a source of clock voltage pulses 24 is used for the addressing, the falling edge of each pulse 24 being used to clock the shift register 6 and the rising edge of each pulse 24 being used to trigger the reset gate 5.

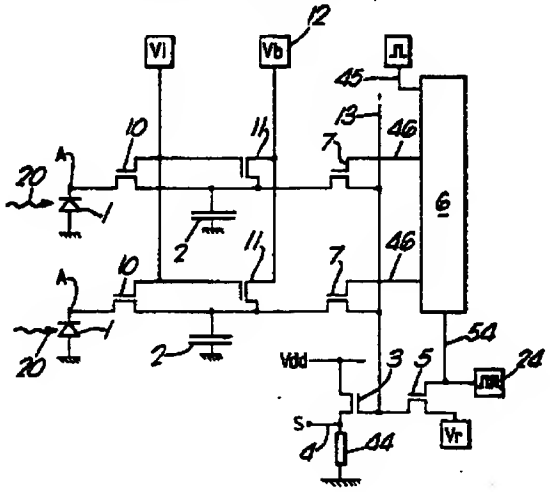

Fig .1.

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Fig .1.

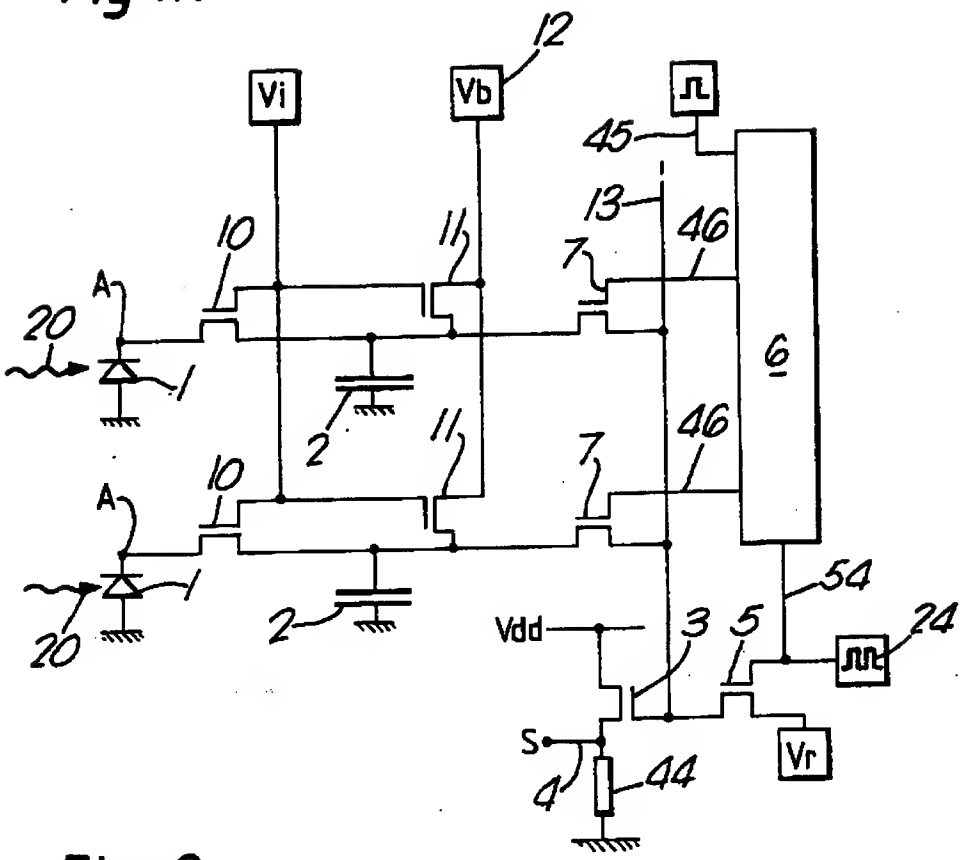
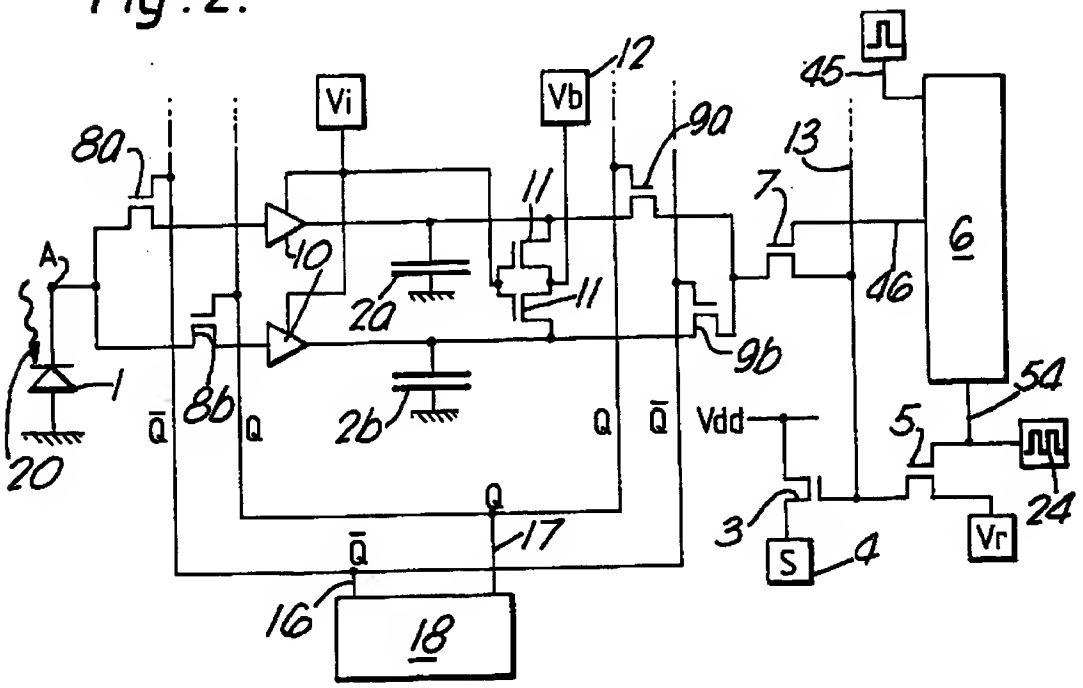

Vi
Vb
12
45
13
46
7
10
11
A
20
1
2
6
54
24
Vdd
3
5
S
4
44
Vr

Fig .2.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Vb
12
45
80
90
13
7
11
A
40
20
6
46
1
8b
9b
54
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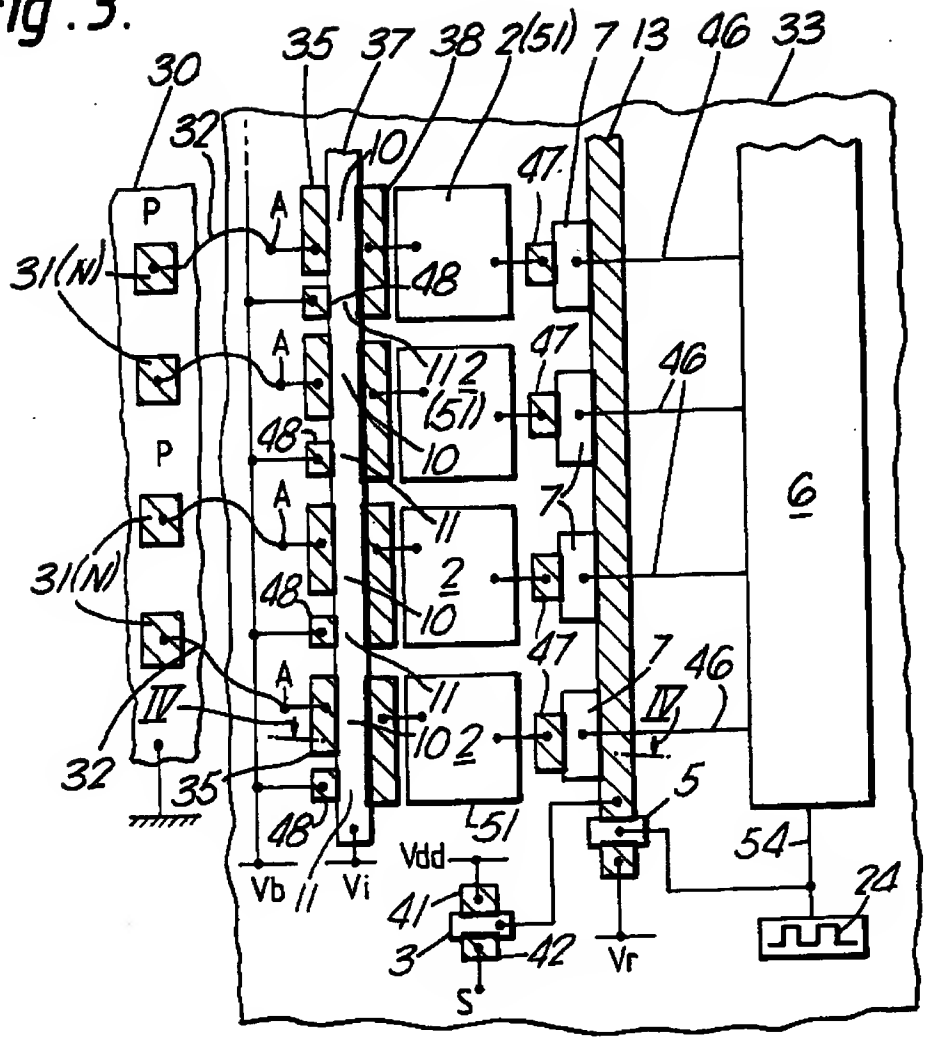
Q
2b
Vdd
5
3
S
4
Vr
24
17
16
18

Fig.3.


30
35
37
38
2(51)
7
13
46
33
32
10
47
P
A
31(N)
48
112
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IV
5
54
24
Vdd
Vb
Vi
41
3
42
Vr
S

Fig.4.

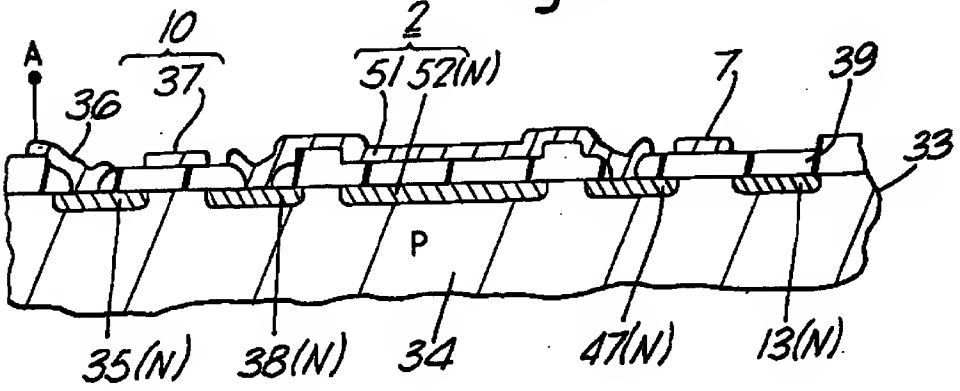
A
10
37
2
51
52(N)
7
39
36
33
P
35(N)
38(N)
34
47(N)
13(N)

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Fig. 5.

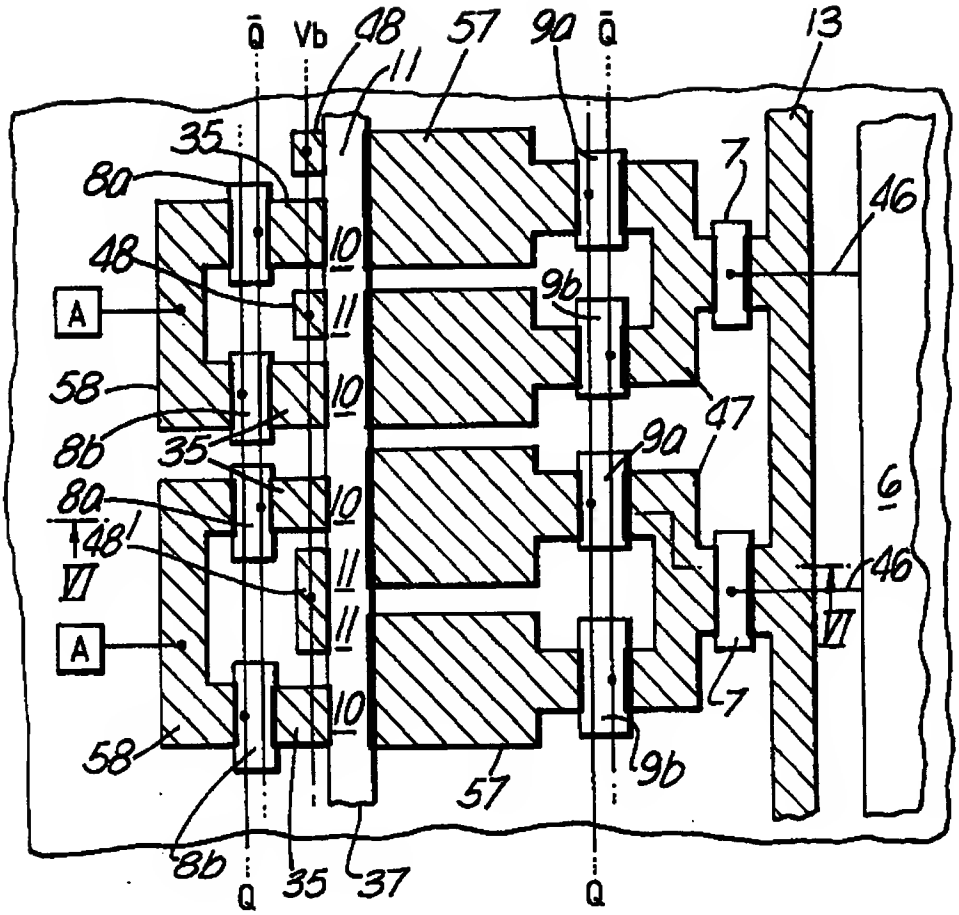


Fig. 6.

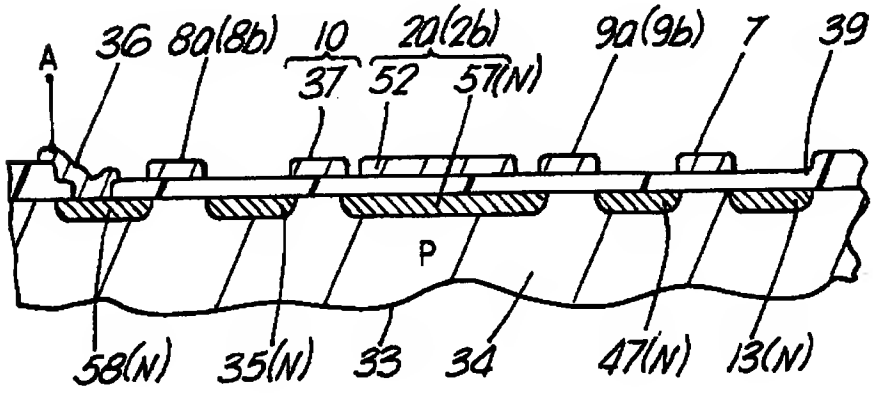


Fig. 7.

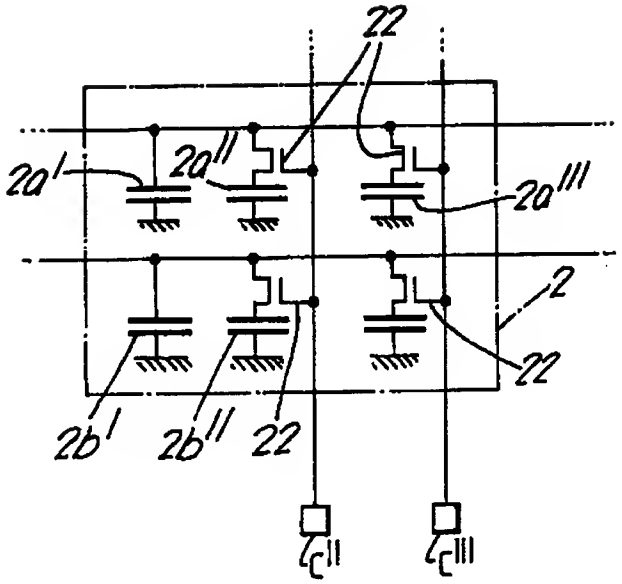
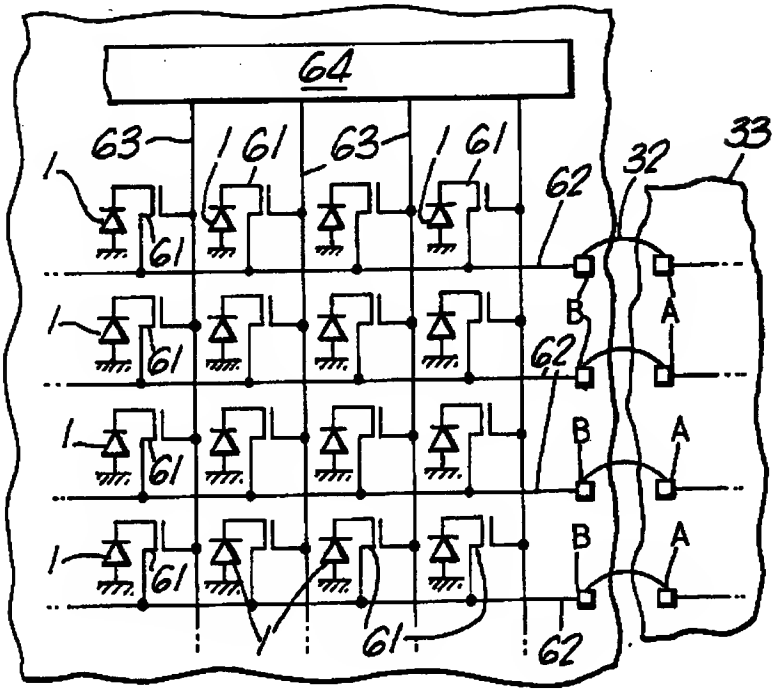


Fig. 8.



SPECIFICATION

Infrared Imaging devices

This invention relates to infrared imaging devices, particularly but not exclusively so-called hybrid devices which may comprise infrared detector elements of, for example, of cadmium mercury telluride coupled to capacitor means in, for example, a silicon circuit body. Such devices may be used in so-called "solid-state" video cameras operating at infrared wavelengths, for example in the 3 to 5 μm (micrometres) or 8 to 14 μm bands.

In European patent application (EP—A) 0 128 828, there is disclosed an infrared imaging device comprising (a) a plurality of infrared detector elements which generate photocurrent in response to incident infrared radiation, (b) capacitor means coupled to each detector element for integrating the current at that detector element during an integration period, (c) voltage-reading means coupled between the capacitor means and a signal output to produce an output signal by reading the potential at said capacitor means which corresponds to the current integrated at the capacitor means, (d) reset means coupled to the capacitor means for resetting the capacitor means to a reference voltage level before the beginning of each integration period, and (e) addressing and switching means permitting said output signals corresponding to the plurality of detector elements to occur sequentially at the signal output and permitting the capacitor means of the detector element to be sequentially reset.

Such an imaging device differs in its features (b) to (e) from previous imaging devices using charge-coupled devices (CCDs) for processing and reading the signals from the detector elements. In particular by integrating the detector element current in such resettable capacitor means and by reading the capacitor potential using such voltage-reading means, it is possible to avoid certain disadvantages of charge-coupled devices in requiring high operating voltages, in introducing charge-transfer noise between successive stages of the CCD and in limiting the signal handling capability to values which are sometimes significantly less than what is desirable particularly for infrared imaging. Furthermore, the technology for fabricating CCDs is more complex than MOS transistor technology (for example, *n* channel MOST technology) with which the signal processing circuit of this type of imaging device can be fabricated.

However, an essential feature of all the imaging devices disclosed in EP—A—0 128 828 is that each cell (formed by a capacitor means coupled to a detector element) is provided with its own voltage-reading means (for example a source-follower MOS transistor M11, M21, M31, M41 in Figure 1 of EP—A—0 128 828) which is individually sequentially switched (for example by an addressing MOS transistor M12, M22, M32, M42 in Figure 1 of EP—A—0 128 828). For this reason considerable care is needed in the fabrication of the device to ensure good uniformity in characteristics between the individual voltage-reading means of the cells at different locations so as to avoid different output signals being produced by different voltage-reading means for the same value of signal from different detector elements. In most of the device arrangements disclosed in EP—A—0 128 828, currents from the individual voltage-reading transistors (for example M11) are switched by the individual addressing transistors (for example M12) to a common load MC of the device at the signal output. Significant non-uniformity in characteristics and hence output signals may result from fabrication inhomogeneities in the circuit body at locations remote from the common load. Such non-uniformity may result in a fixed spatial pattern of noise in the imaging device which may reduce the detectable contrast over a part of the image.

Figure 5 of EP—A—0 128 828 describes a modification which may reduce the effect of such non-uniformities, by providing each cell with an individual load (M1C, M2C) the signal across which is switched individually to the output by the individual addressing transistors (M12, M22). However, this modification multiplies the power dissipation in the device by the number of cells and so renders it more difficult to cool the device to cryogenic operating temperatures. The number of circuit elements associated with each cell and so occupying space on the signal processing circuit body is also increased.

EP—A—0 128 828 also discloses the use of individual reset means (for example MOS transistors M13, M23, M33, M43 in Figure 1) associated with each cell and in particular discloses an interconnection of the individual cell switching means (for example M22) with the individual reset means (for example M13) of the preceding cell so that as the voltage from one cell is read the preceding cell is reset. This provides a simple automatic arrangement for resetting the preceding cell, but it has been noted by the present inventor that when there is a variation in the supplied reset voltage (due to noise or interference, for example) a corresponding variation of the output signal can result when the reset cell is subsequently read. This output signal is measured with respect to the earth potential to which the load MC is connected in the devices of EP—A—0 128 828.

Since the integration time for the imaging devices in EP—A—0 128 828 excludes the reset time, the signals from different detector elements are integrated at different times so that the detector elements do not stare coincidentally.

Although mostly linear arrays of detector elements are described, the capacitor means, voltage-reading means and reset means disclosed in EP—A—0 128 828 can be used with a two-dimensional array. However, as illustrated in Figure 3 of EP—A—0 128 828 this leads to the provision of a corresponding number of individual voltage-reading means and reset means in a two-dimensional array which can occupy a large area of the signal processing circuit body.

According to the present invention, there is provided an infrared imaging device comprising (a) a plurality of infrared detector elements which

generate photocurrent in response to incident infrared radiation, (b) capacitor means coupled to each detector element for integrating the current generated at that detector element during an integration period, (c) voltage-reading means coupled between the capacitor means and a signal output to produce an output signal by reading the potential at said capacitor means which corresponds to the current integrated at the capacitor means, (d) reset means coupled to the capacitor means for resetting the capacitor means to a reference voltage level before the beginning of each integration period, and (e) addressing and switching means permitting said output signals corresponding to the plurality of detector elements to occur sequentially at the signal output and permitting the capacitor means of the detector elements to be sequentially reset, the device being characterised in that the voltage-reading means and the reset means are each common for the plurality of detector elements, and in that the capacitor means of each detector element is switchably coupled by means of the addressing and switching means to both said common voltage-reading means and said common reset means so as to switch each capacitor means sequentially to the common voltage-reading means and to reset sequentially the reference voltage level at each capacitor means and at the common voltage-reading means.

The present invention is based on a recognition by the present inventor that, in such an imaging device, common voltage-reading means and common reset means may be advantageously adopted to avoid problems with non-uniformity of individual voltage-reading means, permit the output signal to be read with respect to the reference voltage level of the common reset means so compensating for variations in the reset voltage supply, and provide a compact circuit element structure for reading and resetting all the capacitor means so that the signal processing circuitry may either occupy a smaller semiconductor circuit body or may advantageously include further circuit elements to improve or extend the device performance (for example, blooming-protection means, or an expanded capacitor arrangement for increasing or varying the integration capacity and/or for providing alternately switchable integration means for each detector element). Furthermore, such a signal-processing circuit having common voltage-reading means and common reset means can be interfaced in a compact arrangement with a switchable two-dimensional array of detector elements. Furthermore, it is possible to access the individual detector elements through the common reset means and the addressing and switching means so that the characteristics of the individual detector elements can be measured during the testing of the device.

In such a device in accordance with the invention, the capacitor means is switched to the voltage-reading means, rather than switching the voltage-reading means to the output as in EP—A—0 128 828.

The capacitor means of the detector elements may be located in a row beside and switchably coupled to a common signal line at a location along which the common voltage-reading means and common reset means are connected, and an injection gate for controlling injection of the current from the detector element to the capacitor means may be located on the other side of the row of capacitor means and may extend parallel to the common signal line. This provides a particularly convenient layout for a compact circuit structure.

The common voltage-reading means may simply be formed by a source-follower insulated-gate field-effect transistor, the insulated gate of which is connected to the common signal line. When the common signal line is formed at least partly as a deposited metallization layer, a part of this metallization layer may be extended over a thin insulating layer between source and drain zones to provide the insulated gate. When the common signal line is formed as a doped semiconductor zone, the insulated gate of the voltage-reading transistor can be connected to the doped zone at a conveniently located contact window. Instead of an insulated-gate transistor, a junction-gate field-effect transistor may be used for the voltage-reading means, but this may complicate undesirably the fabrication of the circuit. The transistor forming the common voltage-reading means may be provided towards one end of the common signal line so as to simplify the layout. This is particularly advantageous when the common signal line is sandwiched between the capacitor means and other circuitry such as a shift register or a decoder used to address the switching means.

The common reset means may conveniently comprise an insulated-gate field-effect transistor the source and drain of which are connected between the common signal line and a reference-voltage supply means. When the common signal line is formed at least partly by a doped semiconductor zone, the source and drain may be formed as interrupted portions of that zone with an insulated gate therebetween to form the transistor. The source and drain of the transistor forming the common reset means may be connected between one end of the common signal line and the reference-voltage supply means so as to simplify the layout.

Various known forms of addressing and switching means may be used to switchably couple each capacitor means to the common voltage-reading means and to the common reset means. In a presently preferred form, said addressing and switching means comprises a shift register having sequential outputs which are connected to a plurality of insulated gates located between the capacitor means and a common signal line, which insulated gates when sequentially addressed from the shift register switchably couple the capacitor means of the detector elements sequentially to the common signal line. A decoder circuit may be employed instead of a shift register. One advantage of using a shift register is that a source of clock voltage pulses may be connected to both a gate of said reset means and an input of the shift register,

the rising edge of each pulse may be used to trigger the gate of said reset means, and the falling edge of each pulse may be used to clock the shift register so as to trigger the switchable coupling of the capacitor means of each detector element sequentially to the common voltage-reading means. This provides a particularly simple means for rapidly and automatically resetting the capacitor means for a well-defined time determined by the duration of the pulse.

As mentioned hereinbefore, the simplification of the circuitry by providing common voltage-reading means and common reset means permits the inclusion of further circuit elements to improve or extend the device performance.

In one such form, the capacitor means of each detector element may comprise at least two capacitors connected in parallel, and at least one of the capacitors may have means permitting its connection to or disconnection from the other(s) so permitting a higher or lower total storage capacity to be obtained when so desired for the device application. This provides a more versatile signal processing circuit and can increase the dynamic range of the imaging device. Thus, increased storage capacity obtained by connecting two or more capacitors in parallel may be used when looking at a hotter scene or when looking (i.e. integrating) for a longer time with the same scene both of which result in an increased signal from the detector elements. Another situation in which this facility can be useful is the fabrication of imaging devices operating at different infrared wavelengths. Thus, for example a large signal can generally be obtained from a scene with cadmium mercury telluride detector elements designed to operate in the 8 to 14 μm wavelength band rather than the 3 to 5 μm wavelength band. This variable capacitance facility permits either type of detector element to be coupled to the capacitor means in a device in accordance with the invention.

Another form of further circuit elements which may be included advantageously in a device in accordance with the invention is blooming-protection means coupled to each capacitor means to inhibit inversion of the potential of the capacitor means when the current generated at the detector element exceeds a level sufficient to discharge fully the capacitor means. No such anti-blooming means were provided in the devices disclosed in EP—A—0 128 828. The blooming-protection means may comprise a further gate which has substantially the same threshold voltage as an injection gate between the detector element and the capacitor means, and this further gate may be connected at substantially the same control potential as the injection gate so as to become activated when the capacitor means becomes fully discharged by excessive current generated at the detector element. This further gate when activated can couple the capacitor means to a source supplying compensating current to the capacitor means to stabilize the potential of the capacitor means and of its detector element by compensating for the excess current generated by the detector element. The injection gates and the further gates may be formed simply as alternate integral parts of a common gate stripe extending at one side of a row of the capacitor means.

In a further form, instead of employing a single capacitor for each detector element as in the imaging devices of EP—A—0 128 828, first and second capacitor means may be switchably coupled in alternate parallel arms between each detector element and a signal line to the common voltage-reading means, the switchable coupling being by means of a switching arrangement which has input gates from the detector element and output gates to the signal line. This permits one of the first and second capacitor means to be coupled to the detector element but isolated from the voltage-reading means while the other of the first and second capacitor means is coupled to the voltage-reading means but isolated from the detector element. Thus each detector element can be operated the whole time for infrared detection without its signal being lost (i.e. not integrated) when reading the previous output signal from that detector element, and all the detector elements can stare at the scene at the same time.

It is particularly convenient to arrange in a row the capacitor means in a device in accordance with the present invention. This is readily compatible with coupling the capacitor means to a linear array of detector elements. However, as mentioned hereinbefore, the signal processing circuitry of an imaging device in accordance with the present invention can be interfaced to a plurality of detector elements arranged as a two-dimensional array. The detector elements may be switchably connected via respective switches in a two-dimensional array of switches to signal paths which are coupled to the capacitor means at least via input gates.

These and other features in accordance with the invention will be illustrated more specifically in embodiments of the invention now to be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a circuit diagram of an infrared imaging device in accordance with the invention;

Figure 2 is a circuit diagram of a modification of the device of Figure 1 which includes alternately switchable storage capacitors for each detector element;

Figure 3 is a plan view of one possible layout for part of the device of Figure 1;

Figure 4 is a cross-section on the line IV—IV of Figure 3 showing one form of integrated circuit technology which may be used to fabricate the signal-processing circuitry part of the device of Figure 1;

Figure 5 is a plan view of part of the layout of Figure 3, modified to provide alternately switchable storage capacitors as in Figure 2;

Figure 6 is a cross-section on the line VI—VI of Figure 5;

Figure 7 illustrates a further modification of the capacitor means for a detector element of the device, and

Figure 8 is a circuit diagram of a two-dimensional

array of detector elements and switches which may be incorporated as a modification at least in the device of Figure 2.

It should be noted that all these Figures are diagrammatic. The plan and sectional views of Figures 3, 4, 5 and 6 are not drawn to scale but the relative dimensions and proportions of parts of these Figures have been shown exaggerated or diminished for the sake of clarity and convenience in the drawings. The same reference signs as used in one embodiment are generally used when referring to corresponding or similar parts in other embodiments.

The infrared imaging device of Figure 1 comprises a plurality of infrared detector elements 1 which generate photocurrent in response to incident infrared radiation 20. Capacitor means 2 are coupled to each detector element 1 for integrating the current generated at that detector element 1 during an integration period. An injection gate 10 controls injection of the current from the detector element 1 to the capacitor means 2. Voltage-reading means 3 are coupled between the capacitor means 2 and a signal output 4 to produce an output signal S by reading the potential at the capacitor means 2 corresponding to the amount of current integrated at the capacitor means 2. Reset means 5 are coupled to the capacitor means 2 for resetting the capacitor means 2 to a reference voltage level Vr before the beginning of each integration period. Addressing and switching means 6, 7 permit the output signals S corresponding to the plurality of detector elements 1 to occur sequentially at the signal output 4 and permit the capacitor means 2 of the detector elements 1 to be sequentially reset. In accordance with the present invention, the voltage-reading means 3 and the reset means 5 are each common for the plurality of detector elements 1, and the capacitor means 2 of each detector element 1 is switchably coupled by means of the addressing and switching means 6, 7 to both the common voltage-reading means 3 and the common reset means 5 so as to switch each capacitor means 2 sequentially to the common voltage-reading means 3 and to reset sequentially the reference voltage level Vr at each capacitor means 2 and at the common voltage-reading means 3.

This form of device illustrated in Figure 1 and having common voltage-reading means and common reset means presents a significant improvement in performance over the devices disclosed in EP—A—0 128 828 having individual voltage-reading means and individual reset means for each capacitor means. Because the device of Figure 1 does not have these individual circuit elements associated with each capacitor means, it is much easier (in terms of layout and body area) to incorporate further circuit elements in accordance with the present invention into the Figure 1 form of device rather than into those disclosed in EP—A—0 128 828. Examples of such further circuit elements illustrated in the drawings are blooming-protection means 11 and 12, first and second capacitor means 2*a* and 2*b* (see Figure 2) switchably coupled in alternate parallel arms between each detector element 1 and the voltage-reading means 3, and plural capacitors 2a', 2a'', 2a''' (see Figure 5) switchably connected for allowing a higher or lower total storage capacity to be provided.

The drawings only show, for the sake of convenience, a small number of detector elements 1 and their signal processing. However, in practice, these imaging devices will have a large number of such detector elements 1 and corresponding signal processing circuitry. Thus, the devices of Figures 1 and 2 may be used in infrared video cameras having, for example, linear arrays of 32 or 64 or even 128 detector elements 1 across which the scene which is being viewed in the infrared is imaged and raster-scanned in known manner by means of lenses and progressively stepped reflectors. Depending on the type of camera and imaging system, the scan direction may be in the longitudinal direction of the linear array or perpendicular to that direction.

The detector elements 1 may be photovoltaic diodes of known type formed in a common body 30 (see Figure 3) of cadmium mercury telluride, the composition of which can be chosen for operation in, for example, the 3 to 5 μm waveband or the 8 to 14 μm waveband. The bulk of the body 30 may be of *p* type material at the detector operating temperature, for example 70°K for the 8 to 14 μm waveband. Each detector element may comprise an *n* type region 31 forming a *p-n* diode junction with the *p* type bulk. The common *p* type bulk of the detector elements 1 may be connected to earth potential, and the individual output signals of each photovoltaic element 1 are taken as currents from the *n* type regions 31 via, for example, wire connections 32 to the inputs A of a silicon circuit body 33 containing the signal processing circuitry. For the sake of convenience, Figure 3 does not show electrode metallizations for the *n* type regions 31 and for the *p* type bulk of body 30, but these may be provided in a variety of known manners.

All the signal processing circuitry illustrated in Figures 1 and 2 may be formed in a single circuit body 33. The capacitor means 2 of the detector elements 1 are located in a row and are switchably coupled to a common signal line 13 at a location along which the common voltage-reading means 3 and common reset means 5 are connected. The injection gate 10 of each detector element 1 is located on the other side of the row of capacitor means 2 and extends parallel to the line 13. As shown in Figures 3 and 4, the injection gates 10 may be fabricated as insulated-gate field-effect transistors having separate source zones 35 connected to each input A by electrode connections 36, insulated gates 10 formed by a common gate stripe 37 for the row of capacitor means 2, and separate drain zones 38 for each capacitor means 2. These transistors and, if so desired, the remainder of the signal-processing circuitry in body 33 may be formed using, for example, known *n* channel MOS integrated circuit technology. Thus, source and drain zones 35 and 38 may be *n* type regions in a *p* type portion of the silicon body 33, the individual transistors are isolated from each other in known

mennar at active areas defined by a thick field oxide layer 39 at the body surface, whlie e much thinner insulating layer is present below the active ereas of the gates formed by tracks of, for example, doped polycrystalline silicon or e metal silicide.

In the form shown by way of example in Figures 3 to 6, the common signal line 13 is an *n* type stripe in the *p* type portion of the silicon body 33. In thie case, the reset gate 5 can be a transistor switch formed by an insuleted gate over e gap in the *n* type stripe 13 the interrupted parts of which provide the source and drain of the trensistor, for example at one end of the line 13. In the plan views of Figures 3 and 5, *n* type regions ere hetched, whereas insulated gate erees ere unhatched. Tha common voltage-reading means 3 is (as shown in Figures 1 and 2) a eource-follower field-effect transistor having an insulated gate 43 connected to the common signal line 13, an *n* type drain zone 41 connected to a voltage supply line Vdd (for example, at about 9 volts), and an *n* type source zona 42 connected to earth potential via e loed transistor 44. Thie load 44 may be an *n* channel field effect transistor whose insulated gate and source ere connected together in known manner. For the sake of convenience thia load transistor structure is not shown in Figure 3. The signel output 4 of the devices of Figures 1 end 2 is taken from the source zone 42 of the common voltage-reading transistor 3. An emplifier (which may also be formed in tha body 33) may be connected to this output 4 to amplify the output eignal S.

The addressing end sequential switching of the capacitor means 2 to the common aignal line 13 is effected by means of a high speed shift register 6 having sequential outputs 46 connected to a plurality of insulated gates 7 located between the capacitor means 2 and the signal line 13. These gates 7 may be fabricated as transistor structures illustrated in Figures 3 to 6 having *n* type individual source zones 47 end a common drain zone formed by the *n* typa signal line 13. The sequence of outputs 46 from the shift register 6 includes en initial (or final) output 45 which provides a line synchronisation pulse for the devlce signal S when the sequentially shifted output pulse from the register 6 appears at the output 45.

The capacitor means 2 for temporarily storing and integrating the charge signels from the detector elements 1 may be constructed in verious ways. Thus, for example, using *n* channel MOS integrated circuit technology, the separately-connected storage plates of the individual capacitors may be formed by separate *n* type regions (for example regions 57 of Figures 6 and 7) but insulated from an overlying insuleted gate stripe which is common for all the capacitors and which is connected to earth potential. However, the capacitance of the capacitor constructed in this way also includes that of the *p-n* junction between the *n* typa region and the *p* type body portion 34, end this *p-n* junction capacitance varies with voltage. Figures 3 end 4 illustrate an inverted construction in which the seperately-connected storage plates ere insulated gate areas each connected between *n* typa side regions formed by a drain region 38 of an injection gate transistor end en *n* type source region 47 of en addressing transistor 7. In this case there ie a common *n* type stripe 52 which forms the bottom plate of the capacitors 2 and which is connected to earth potential. Thie construction is more complicated and may occupy more spece, but its capacitance is much more stable with voltege. It is also possible to form the capacitor 2 wholly deposited on the surface of the body 33, for example as e metal plate deposited on a dielectric leyer on a polycrystalline silicon layer in the insulating leyer 39.

Due to its advantageous design, the operation of the device end circuit of Figure 1 Is comperatively simple. A low constant voltage Vi (for example, about 1 volt) is applied to tha injection gates 10 to operate the input transistors 35—10—38 in known manner in the condition where the channel current of the transistor is controlled by the gate-to-source voltage so as to equel the detector element photocurrent, thereby meintaining the detector elements 1 in a zero-bias condition. In this way the injection gates 10 serve to stabilize the operation of the photodiodes 1 illuminated by the redietion 20.

The injected current aignal ia integrated on the capacitor 2. For this purpose, the capacitor 2 Is charged before the beginning of the integration period by resetting its potentiel to the reference level Vr (for example, about 5 volts), after which it is isoleted from the line 13 for the Integration period. Tha capacitor 2 becomes at least partially discharged during the integration period by the current signal from the detector elements. The potential corresponding to the charge state of each capacitor 2 at the end of its integration period is read by coupling that capacitor 2 vie its addressing gata 7 to the gata of the source-follower transistor 3. Tha injection gates 10 protect the detector elements 1 from the effects of reading and resetting their capacitor means 2. The gates 7 ere sequentially addressed by an output pulse which appears sequentially on the outputs 46 of tha shift register 6. In tha arrangement illustrated In Figures 1 end 2, a source of clock voltage pulses 24 is connected to both the reset gate 5 end to an input 54 of tha shift register 6. The potential of one capacitor 2 is read in the time interval between the pulses 24.

The threshold voltage of the reset gate 5 is chosen such that the rising edge of each pulse 24 triggers the gate 5 so that the reference voltaga Vr is applied vie the open eddressing gate 7 to that one capacitor 2 which has just been read so reaetting its voltage for its next integration period. At the same time (because the transistor drain of the reset gate 5 is connected to the insulated gate of the source-follower transistor 3) the reference voltage level Vr is also applied to tha transistor 3 so that its output signal S changes from e valua corresponding to the signal from that ona capacitor to a value corresponding to Vr. In thie manner the output signal from each capacitor is measured against the reset voltage level Vr (and not earth potential) so tending to cancel any veriation occurring in the supplied level Vr due to, for example, noise.

The input 54 of the shift register 6 Is so designed

as to cause the falling edge of each pulse 24 to clock the shift register 6 so that the output pulse now appears on the next output 46 in the sequence. This triggers the switchable coupling of the next capacitor 2 in the sequence to the line 13 so that the potential corresponding to the charge state of this next capacitor is read by the source-follower transistor 3.

In the device of Figure 1 is used to view a scene with a very hot spot, the current generated by at least one of the detector elements 1 may exceed a level sufficient to discharge fully the associated capacitor 2, and this excess current could invert the capacitor potential (so that it became negative) in the absence of anti-blooming means 11, 12. The excess current can forward bias the *p-n* junction of this detector element so that it injects electrons into the *p* type bulk of the cadmium mercury telluride body 30 thereby producing an excessive charge signal at least at neighbouring detector elements 1 and possibly along most of the detector element row. However the device of Figure 1 (and that of Figure 2) is protected against such a blooming effect by having a further gate 11 between each capacitor 2 and a source 12 of compensating current to stabilize the potential of the capacitor 2 and its detector element 1.

The further gate 11 has the same threshold voltage as the injection gate 10 and is connected at the same control potential Vi. This is achieved in a simple manner in the layout of Figure 3 by making the injection gates 10 and blooming-protection gates 11 as alternate integral parts of the common insulated gate stripe 37 and by forming source, drain and channel of the transistor structures which provide the injection gate 10 and further gate 11 using the same technology and in the same processing steps. Thus, the gates 11 form part of insulated-gate field-effect transistors each having source and drain formed by a separate *n* type region 48 and an *n* type region 38 which is common with the injection gates 10. Direct coupling between regions 35 and 48 is prevented in known manner by a channel-stop or other form of circuit isolation extending under the parts of the gate stripe 37 between the active gate parts 10 and 11. All these *n* type regions 48 are connected by a metallization track to a supply line at a positive potential (Vb) which may be substantially the same as the reset reference voltage level (Vr), for example 5 volts. Thus, when the associated capacitor 2 is reset the blooming-protection transistor 11 is in a hard off condition due to the significant effective negative potential of its gate, i.e. (Vi-Vr), for example about minus 4 volts, with respect to region 38.

If now a detector element 1 becomes forward biased and the potential of the associated capacitor 2 starts to go negative, the associated region 38 of the blooming-protection gate 11 will start to become negative. As a result, the effective gate potential Vi is now positive with respect to the region 38 so that the blooming-protection transistor formed by the gate 11 will start to conduct so coupling the capacitor 2 to the current supply 12. In this situation the supply 12 provides compensating current to the capacitor 2 to stabilize the potential of both the capacitor 2 and its detector element 1 at about zero volts by compensating for the excess photocurrent. In this way the tendency is avoided for excessive current at a detector element to forward bias the *p-n* junction of that element. However, if so desired, the device of Figure 1 may be constructed without the anti-blooming means 11, 12.

The same basic circuit operation of the device described with reference to Figure 1 occurs in the device of Figure 2, regarding its detector elements 1, injection gates 10, capacitor means 2, blooming-protection gates 11, addressing gates 7, common voltage-reading transistor 3, reset gate 5 and shift register 6. In the device of Figure 2, however, two alternately-switchable capacitors 2*a* and 2*b* are associated with each detector element 1 so that while one capacitor (for example 2*a*) is coupled to the source-follower transistor 3 for reading its potential after integration, the other capacitor (2*b*) is coupled to the detector element 1 for integrating its current signal. The switching arrangement of input gates 8*a* and 8*b* and output gates 9*a* and 9*b* permits each detector element 1 to be operated the whole time for photodetection without its signal being lost (i.e. not integrated) when reading the previous output from that element 1. Therefore, in the device of Figure 2, all the detector elements 1 can stare at the scene at the same time. For the sake of convenience, only one element 1 and the corresponding input A is illustrated in Figure 2.

Each of the first and second capacitors 2*a* and 2*b* may be formed in the same manner as for the device of Figure 1. In the example illustrated in Figures 5 and 6, each capacitor 2*a* or 2*b* comprises an individual *n* type region 57 in the *p* type body portion 34. Each capacitor region 57 is insulated from an overlying metal stripe 52 (not shown in Figure 5) which forms a common top earthed plate of all the capacitors 2*a* and 2*b* and which extends parallel to the injection gate stripe 10. However, if desired, an inverse capacitor structure having a common *n* type stripe 52 (in the body portion 34), and separate insulated gate plates 51*a* and 51*b* connected between *n* type side regions may be provided instead for each capacitor 2*a* and 2*b*, similar to that of Figures 3 and 4. Separate insulated gates 9*a* and 9*b* are present between the *n* type regions 57 and the *n* type region 47 of each addressing transistor 7 to form the alternately switchable output gates. Similarly, instead of the input A being to the *n* type regions 35 of the injection gate transistors 10, each input A is to an *n* type region 58 which is coupled to the individual regions 35 for the capacitors 2*a* and 2*b* by insulated gates 8*a* and 8*b* forming the alternately switchable input gates. It is usually preferable to include the input gates 8*a* and 8*b* between the detector element input A and the injection gate 10 as illustrated in Figures 2, 5 and 6, rather than between the injection gate 10 and the capacitor means 2*a* and 2*b*, because a common injection gate stripe 37 in this latter position may introduce confusion between the input signals from the detector elements 1 due to the large capacitance of the gate stripe 37. Individual

connection regions 48 for the blooming protection means may be provided for each capacitor 2*a* or 2*b*, or e more compect arrangement may be obtalned by having common electrode connection regions 48' located between the gates 11 of each pair of capacitors 2*a* or 2*b*. In practice, either individuel regions 48 or common regions 48' will normelly be used for each pair 2*a* end 2*b* of capacitors in the device; however, both are illustrated for different capacitor pairs in Figure 5 for the sake of convenience, rather than having two drawings.

As illustrated in Figure 2, the switching arrangement 8*a*, 8*b*, 9*a*, 9*b* is controlled by the inverse outputs 16 end 17 of one or more flip-flop circuits 18. One output signal $\overline{Q}$ (from 16) is the inverse of the other Q (from 17). Output 16 is connected to tha input gate 8*a* end to the output gate 9*b*, whereas the output 17 is connected to the gate 8*b* and 9*a*. Thus, when Q is such as to switch on the trensistors having the insulated gates to which it is applied, the capacitor 2*a* is coupled to the detector element 1 to integrate its current output but is isolated from the addressing gate 7 by the off state of the transistor switch having the insulated gate 9*a*, end the capacitor 2*b* is coulpled to the addressing gate 7 but is isolated from the detector element 1 by the off state of the transistor switch having the insulated gate 8*b*.

Figure 7 illustrates a further modification for the capacitor means for each detector element input A. In this form, each of the first and the second capacitor means 2*a* and 2*b* in the alternate parallel erms of the Figure 2 circuit comprises three capacitors (namely 2a', 2a'', 2a''', and 2b', 2b'', 2b''') connected in parallel. At least the capacitors 2a'', 2a''', 2b'' and 2b''' are coupled to the arms via transistor switches 22 the insulated gates of which are connected in pairs to control voltage sources C'' and C'''. This allows each pair of capacitors (either 2a'' end 2b'', or 2a''' end 2b''') to be connected or disconnected from the other(s) so permitting a higher or lower total storage capacity to be obtained when so desired for the device epplication. This arrangement provides e more versatile signal processing circuit and can increase the dynamic range of the Imaging device. The increased storage capacity obtained by connecting two or more capacitors (2e', 2a'', 2a''') in parallel may be used when looking at a hotter scene or even a scene with a hot spot so that this increased storage capacity may even be used in cooperation with the blooming-protection means 11, 12 to cope with excessive current from a detector element 1. Such increased storage capacity may also be employed when looking (i.e. integrating) for a longer time at a scene, since this also results in en increased signal from the detector elements. Another situation in which this fecility can be useful is the fabrication of imaging devices opereting at different infrared wavelengths. Thus, for example a lerge signal (for example up to 30 times more) can generelly be obtained from a scene with cadmium mercury telluride detector elements 1 designed to operate in the 8 to 14 μm wavelength band rather then the 3 to 5 μm wavelength band. This variable capacitance facility (2e', 2a'', 2a''', 2b', 2b'', 2b''', 22) permits either type of detector element 1 to be coupled to the capacitor means 2 in e device in accordence with the invention. Although Figure 7 illustrates three peirs of capacitors, similar devices may be designated with just two such pairs (for example 2a', 2b' end 2a'' and 2b'') for the device of Figure 2, end in the case of Figure 1 the capecitor 2 would be simply repleced by capacitors 2a', 2a'' end, if desired, 2a''' but without pairing.

In the devices so far described with reference to Figures 1 to 7, the row of capacitor means 2 has been coupled to a linear array of detector elements 1. It will be appreciated thet many array variations of the devices of Figures 1 to 6 are possible within the scope of the invention. Thus, for example the detector elements 1 may be arranged in two rows or, for example, an alternately staggering row end may be located between two signal-processing circuit bodies 33, each having a row of capacitor means 2 so that the different rows of detector elements 1 or alternate detector elements 1 may be connected to the different bodies 33. In some devices the detector elements 1 may be provided on or even in the signal-processing circuit body 33. Furthermore, the signal-processing circuitry of imaging devices in accordance with the invention may be interfaced to a two-dimensional array of detector elements 1.

Figure 8 illustrates a two-dimensional erray of photodiode detector elements 1 which are switchebly connected via respective switches 61 to signals paths 62. Although only sixteen detector elements 1 and switches 61 are shown in Figure 8, there will usually be meny more, for exemple at least a 64 × 64 array or 128 × 128 array. The switches 61 may be insulated-gate field-effect transistors and are arranged in e two-dimensional array corresponding to that of the detector elements 1. Once egeln, the detector elements 1 may be of cadmium mercury telluride end they may be mounted by a variety of known techniques on a silicon circuit body comprising the switches 61 and signel paths 62. Two exampies of suitable mounting end interconnection technologies are described in European patent application EP—A—0 061 803 (our reference PHB 32767) which describes the formation end connection of ennular *n* type detector element regions around the side-walls of apertures in e *p* type body on a silicon circuit substrate, and in I.E.E.E. 1978 International Electron Devices Meeting, Weshington D.C., pages 510 to 512 which describes indium bump connections between detector element regions at the bottom surface of an opposite conductivity type body also on e silicon circuit substrate.

The transistors 61 in each (horizontal) column ere sequentielly switched on by a pulse appearing sequentially on the outputs 63 of a shift register 64 which may be integrated into the same silicon circuit body as the switches 61. By this means, the detector elements 1 in each column are switched sequentially to the row of outputs B of the paths 62 which are connected to the inputs A of e signel processing circuit such es that shown in Figure 2.

When the array of Figure 8 is connected to the circuit of Figure 2, the signals from one line (vertical row) of detector elements 1 may be read from, for exmaple, the capacitors 2*a* by the source-follower transistor 3 while the signals from the next line (vertical row) of detector elements 1 are being coupled to and integrated in the capacitors 2*b*. Thus, this imaging device has a line equivalent performance from each row of the two-dimensional array, with the same stare time (and integration time) for each detector element 1 in the line (vertical row). Since the individual switching transistors 61 and their connections can be fabricated with a very compact geometry it is possible to provide a large number of switches 61 and detector elements 1 in a closely packed array so that much larger arrays (in small areas) and higher spatial resolutions can be achieved with the imaging device of Figures 2 and 8, as compared with both CCD imaging devices and the Figure 3 device of EP—A—0 128 828.

The array of Figure 8 may be connected to the circuit of Figure 1, if a pulse is applied to the injection gate 10 so as to isolate the capacitor 2 from the input A when its potential is being read by the transistor 3. However, the time for staring/integration would then be reduced by the time taken for scanning the line.

CLAIMS

1. An infrared imaging device comprising (a) a plurality of infrared detector elements which generate photocurrent in response to incident infrared radiation, (b) capacitor means coupled to each detector element for integrating the current generated at that detector element during an integration period, (c) voltage-reading means coupled between the capacitor means and a signal output to produce an output signal by reading the potential at said capacitor means which corresponds to the current integrated at the capacitor means, (d) reset means coupled to the capacitor means for resetting the capacitor means to a reference voltage level before the beginning of each integration period, and (e) addressing and switching means permitting said output signals corresponding to the plurality of detector elements to occur sequentially at the signal output and permitting the capacitor means of the detector elements to be sequentially reset, characterised in that the voltage-reading means and the reset means are each common for the plurality of detector elements, and in that the capacitor means of each detector element is switchably coupled by means of the addressing and switching means to both said common voltage-reading means and said common reset means so as to switch each capacitor means sequentially to the common voltage-reading means and to reset sequentially the reference voltage level at each capacitor means and at the common voltage-reading means.

2. A device as claimed in Claim 1, further characterised in that the capacitor means of the detector elements are located in a row beside, and are switchably coupled to, a common signal line, that the common voltage-reading means and common reset means are connected at a location along the common signal line, and that an injection gate for controlling injection of the current from the detector element to the capacitor means is located on the other side of the row of capacitor means and extends parallel to the common signal line.

3. A device as claimed in Claim 2, further characterised in that the common voltage-reading means is formed by a source-follower insulated-gate field-effect transistor, the insulated gate of which is connected to the common signal line.

4. A device as claimed in Claim 3, further characterised in that the transistor forming the common voltage-reading means is provided towards one end of the common signal line.

5. A device as claimed in any one of Claims 2 to 4, further characterised in that the common reset means comprises an insulated-gate field-effect transistor the source and drain of which are connected between the common signal line and a reference-voltage supply means.

6. A device as claimed in Claim 5, further characterised in that the source and drain of the transistor forming the common reset means are connected between one end of the common signal line and the reference-voltage supply means.

7. A device as claimed in any one of the preceding Claims, further characterised in that said addressing and switching means comprises a shift register having sequential outputs which are connected to a plurality of insulated gates located between the capacitor means and a common signal line, which insulated gates when sequentially addressed from the shift register switchably couple the capacitor means of the detector elements sequentially to the common signal line.

8. A device as claimed in Claim 7, further characterised in that a source of clock voltage pulses is connected to both a gate of said reset means and an input of the shift register, the rising edge of each pulse being used to trigger the gate of said reset means and the falling edge of each pulse being used to clock the shift register so as to trigger the switchable coupling of the capacitor means of each detector element sequentially to the common voltage-reading means.

9. A device as claimed in any one of the preceding Claims, further characterised in that the detector elements are of cadmium mercury telluride, and the capacitor means, voltage-reading means, reset means, and addressing and switching means are formed in at least one silicon circuit body.

10. An infrared imaging device having any of the novel features described herein and/or illustrated with reference to any of the accompanying drawings.

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